IN THE CLAIMS:

1. (Original) A method, comprising:

receiving a pair of input clock signals;

utilizing a stratum clock state machine to control a multiplexer;

utilizing the multiplexer to switch an input of a main clock between each of the pair of input clock signals;

inducing a phase build-out activity; and

transmitting an output clock signal.

2. (Original) The method of claim 1, wherein inducing the phase build-out activity includes eliminating a set of input transients.

3. (Original) The method of claim 1, further comprising utilizing the stratum clock state machine to manage a plurality of phase-locked loops.

4. (Original) The method of claim 1, further comprising utilizing the stratum clock state machine to set the main clock to a main clock normal state

5. (Original) The method of claim 1, further comprising utilizing the stratum clock state machine to set the main clock to a main clock freerun state.

6. (Original) The method of claim 1, further comprising utilizing the stratum clock state machine to set the main clock to a main clock holdover state.

7-14. Canceled

15. (Original) The method of claim 1, further comprising setting the stratum clock state machine in a state including at least one member selected from the group consisting of: a

stratum clock state machine normal state, a stratum clock state machine freerun state, a stratum clock state machine switch state, a stratum clock state machine offset state and a stratum clock state machine holdover state.

16-26. Canceled

27. (Original) A computer program, comprising computer or machine readable program elements translatable for implementing the method of claim 1.

28. (Original) An apparatus for performing the method of claim 1.

29. (Original) A field programmable gate array for performing the method of claim 1.

30. (Original) An application specific integrated circuit for performing the method of claim 1.

31-48. Canceled